LAMPIRAN

www.p-tec.net
sales@p-tec.net

Tel: (719) 589 3122
Fax: (719) 589 3592

PC1602A-L (16x2) Character LCD Display

Features

*16 Character, 2 Line
*View Angle 12H or 6H
*TN or STN Fluid
*Extended Temperature Range available
*Several Character Types available
*LED or EL Backlight available

Absolute Maximum Ratings at T_A = 25 °C

Item	Symbol	Min	Max	Unit
Power Supply (Logic)	Vdd	-0.3	7.0	V
Power Supply (LCD)	Vo	Vdd – 0.3	Vdd 12.0	V
Input Voltage	Vi	- 0.3	Vdd	V
Operating Temperature (Standard)	Topr	0	50	°C
Storage Temperature (Standard)	Tstg	- 20	70	°C
Extended Operating Temperature	Topr	- 20	70	°C
Extended Storage Temperature	Tstg	- 30	80	°C

Electrical Characteristics at T_A = 25 °C, Vdd=5V+0.25V

Item	Symbol	Min	Typ	Max	Unit
Power Supply (Logic)	Vdd-Vss	4.7	5.0	5.3	V
Supply Current	Idd	—	2.0	3.0	mA
LCD Driving Voltage	Vdd -Vo	4.2	4.5	4.8	V
Input Voltage "H"	Vih	2.2	—	Vdd	V
Input Voltage "L"	Vil	—	—	0.6	V
Output Voltage "H"	Voh	2.4	—	—	V
Output Voltage "L"	Vol	—	—	0.4	V

Interface Pin Connection

No	Symbol	Function	No	Symbol	Function
1	Vss	Power Supply (GND)	9	DB2	Data Bus Line 2
2	Vdd	Power Supply (+5V)	10	DB3	Data Bus Line 3
3	Vo	Contrast Adjust	11	DB4	Data Bus Line 4
4	RS	Instruction/Register Select	12	DB5	Data Bus Line 5
5	R/W	Read/Write	13	DB6	Data Bus Line 6
6	E	Enable Signal	14	DB7	Data Bus Line 7
7	DB0	Data Bus Line 0	15	A	Power Supply for LED Backlight (+)
8	DB1	Data Bus Line 1	16	K	Power Supply for LED Backlight (-)

LED Backlight Specifications

Forward Voltage	Forward Current	Power Dissipation	Peak Wavelength
4.2V (Typ)	195mA (Max)	900mW (Max)	570nm (Typ)

Mechanical Specifications

Item	Overall Size	Viewing Area	Character Size	Character Pitch	Dot Size
Specifications	80.0W x 36.0H x 8.8T (BL12.7T)	65.0W x 16.0H	2.96W x 5.56H	3.55W x 5.94H	0.56W x 0.66H

All dimensions are in mm. Tolerance is ± 0.3 Unless otherwise specified

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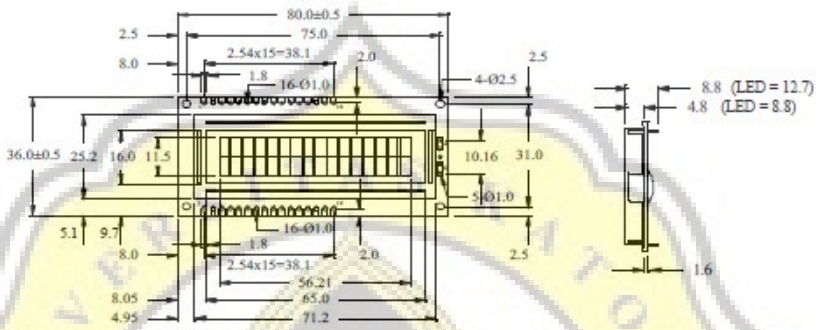
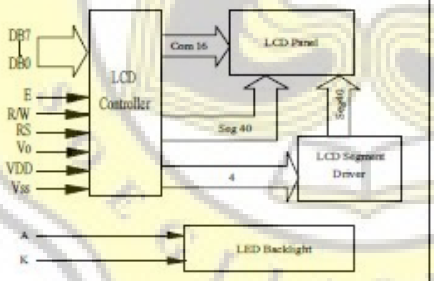
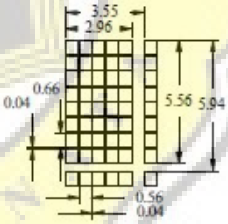
PC1602A-L (16x2) Character LCD Display



LCD Block Diagram



Dot Layout



All dimensions are in mm. Tolerance is ± 0.3 Unless otherwise specified

Micro Commercial Components
20736 Marilla Street Chatsworth
CA 91311
Phone: (818) 701-4933
Fax: (818) 701-4939

MC7805CT

Three-Terminal Positive Voltage Regulators

Features

- Lead Free Finish/RoHS Compliant(Note 1) ("P" Suffix designates RoHS Compliant. See ordering information)
- Output current in excess of 1.0 Ampere
- No external components required
- Internal thermal overload protection
- Internal short-circuit current limiting
- Output voltage offered in 2% tolerance
- Epoxy meets UL 94 V-0 flammability rating
- Moisture Sensitivity Level 1

Maximum Ratings @ T_A=25°C, Unless Otherwise Noted

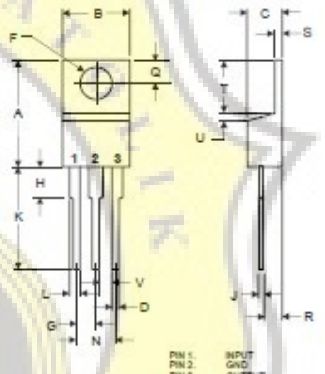
Parameter	Symbol	Value	Unit
Input Voltage	V_I	30	V
Power Dissipation	P_D	15	W
Operating Junction Temperature	T_{OPR}	0----+125	°C
Storage Temperature Range	T_{STG}	-55---+125	°C

Electrical Characteristics (Vi=10V, Io=500mA, 0°C<Tj<125°C, Ci=0.33uF, Co=0.1uF, Unless Otherwise Specified)

Parameter	Sym	Min	Typ	Max	Test conditions
Output Voltage	V_O	4.9V	5.0V	5.1V	T_j=25°C
		4.85V		5.15V	7V≤ V_I ≤20V, 5mA≤ I_O ≤1.0A, P_D=15W
Load Regulation	$\triangle V_O$		15mV	100mV	5mA≤ I_O ≤1.5A, T_j=25°C
			5.0mV	50mV	250mA≤ I_O ≤750mA, T_j=25°C
Line regulation	$\triangle V_O$		3.0mV 1.0mV	100mV 50mV	7V≤ V_I ≤25V, T_j=25°C 8V≤ V_I ≤12V, T_j=25°C
Quiescent Current	I_Q		4.2mA	8.0mA	T_j=25°C, I_O=0
Quiescent Current Change	$\triangle I_Q$			1.3mA 0.5mA	7V≤ V_I ≤25V 5mA≤ I_O ≤1.0A
Output Noise Voltage	V_N		40μV		f=120Hz
Ripple Rejection	RR	62dB	78dB		8V≤ V_I ≤20V f=120Hz, T_j=25°C
Dropout Voltage	V_D		2.0V		I_O=1.0A, T_j=25°C
Output Short Circuit Current	R_O		17mohm		f=1.0KHz
Output Short Circuit Current	I_{OS}		750mA		T_j=25°C
Peak Output Current	I_{OPK}		2.2A		T_j=25°C
Temperature Coefficient of Output voltage	$\triangle V_O$/ $\triangle T_j$		1.1mV/°C		0°C≤ T_j≤ 125°C, I_O=5mA

Notes:1.High Temperature Solder Exemption Applied, see EU Directive Annex 7.

TO-220



DIMENSIONS

DIM	INCHES MIN	INCHES MAX	MM MIN	MM MAX	NOTE
A	.560	.605	14.22	15.88	
B	.380	.420	9.65	10.67	
C	.140	.190	3.56	4.82	
D	.020	.045	0.51	1.14	
F	.139	.161	3.53	4.09	Ø
G	.190	.210	2.29	2.79	
H	---	.250	---	6.35	
J	.012	.025	0.30	0.64	
K	.500	.580	12.70	14.73	
L	.045	.060	1.14	1.52	
N	.190	.210	4.83	5.33	
Q	.100	.135	2.54	3.43	
R	.080	.115	2.04	2.92	
S	.045	.055	1.14	1.39	
T	.230	.270	5.84	6.86	
U	----	.050	----	1.27	
V	.045	----	1.15	----	

MICROCHIP

dsPIC30F4011/4012

dsPIC30F4011/4012 Enhanced Flash 16-bit Digital Signal Controller

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the *dsPIC30F Family Reference Manual* (DS70046). For more information on the device instruction set and programming, refer to the *dsPIC30F Programmer's Reference Manual* (DS70030).

High Performance Modified RISC CPU:

- Modified Harvard architecture
- C compiler optimized instruction set architecture with flexible addressing modes
- 84 base instructions
- 24-bit wide instructions, 16-bit wide data path
- 48 Kbytes on-chip Flash program space (16K Instruction words)
- 2 Kbytes of on-chip data RAM
- 1 Kbytes of non-volatile data EEPROM
- Up to 30 MIPs operation:
  - DC to 40 MHz external clock input
  - 4 MHz-10 MHz oscillator input with PLL active (4x, 8x, 16x)
- 30 interrupt sources
  - 3 external interrupt sources
  - 8 user selectable priority levels for each interrupt source
  - 4 processor trap sources
- 16 x 16-bit working register array

DSP Engine Features:

- Dual data fetch
- Accumulator write back for DSP operations
- Modulo and Bit-Reversed Addressing modes
- Two, 40-bit wide accumulators with optional saturation logic
- 17-bit x 17-bit single cycle hardware fractional/integer multiplier
- All DSP instructions single cycle
- ± 16-bit single cycle shift

Peripheral Features:

- High current sink/source I/O pins: 25 mA/25 mA
- Timer module with programmable prescaler:
  - Five 16-bit timers/counters; optionally pair 16-bit timers into 32-bit timer modules
- 16-bit Capture input functions
- 16-bit Compare/PWM output functions
- 3-wire SPI™ modules (supports 4 Frame modes)
- I²C™ module supports Multi-Master/Slave mode and 7-bit/10-bit addressing
- 2 UART modules with FIFO Buffers
- 1 CAN modules, 2.0B compliant

Motor Control PWM Module Features:

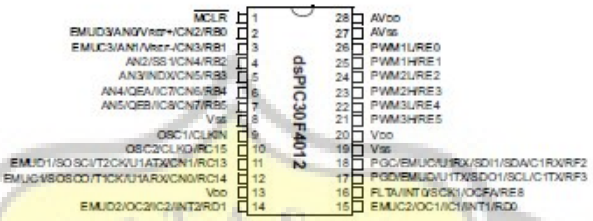
- 6 PWM output channels
  - Complementary or Independent Output modes
  - Edge and Center Aligned modes
- 3 duty cycle generators
- Dedicated time base
- Programmable output polarity
- Dead-time control for Complementary mode
- Manual output control
- Trigger for A/D conversions

Quadrature Encoder Interface Module Features:

- Phase A, Phase B and Index Pulse input
- 16-bit up/down position counter
- Count direction status
- Position Measurement (x2 and x4) mode
- Programmable digital noise filters on inputs
- Alternate 16-bit Timer/Counter mode
- Interrupt on position counter rollover/underflow

Pin Diagrams (Continued)

28-Pin SPDIP
28-Pin SOIC



44-Pin QFN

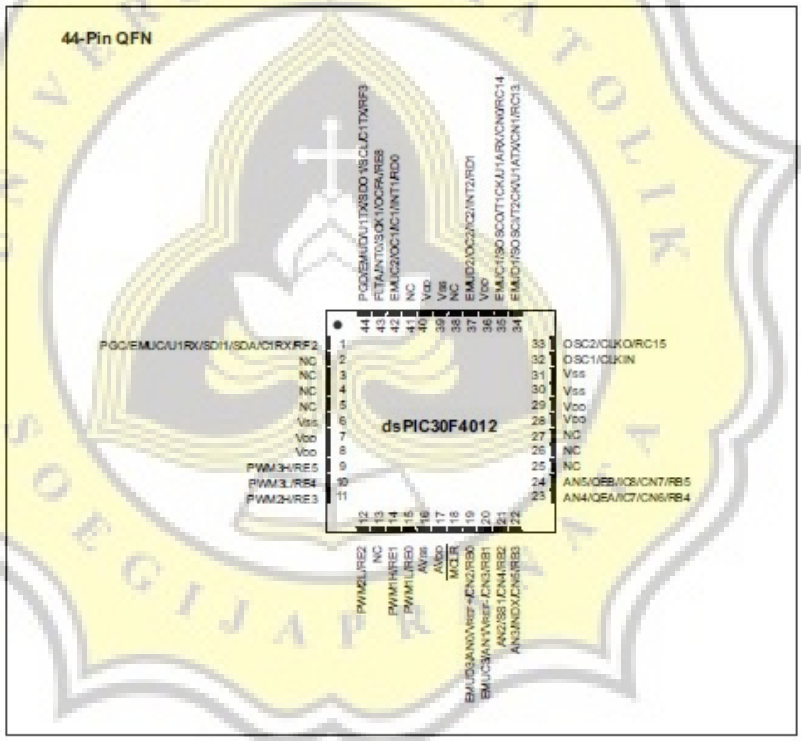


Table 1-2 provides a brief description of the device I/O pinout and the functions that are multiplexed to a port pin. Multiple functions may exist on one port pin. When multiplexing occurs, the peripheral module's functional requirements may force an override of the data direction of the port pin.

TABLE 1-2: dsPIC30F4012 I/O PIN DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	Description
AN0-AN5	I	Analog	Analog input channels. AN0 and AN1 are also used for device programming data and clock inputs, respectively.
AVdd	P	P	Positive supply for analog module.
AVss	P	P	Ground reference for analog module.
CLKI CLKO	I O	ST/CMOS —	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
CN0-CN7	I	ST	Input change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
C1RX C1TX	I O	ST —	CAN1 bus receive pin. CAN1 bus transmit pin.
EMUD EMUC EMUD1 EMUC1 EMUD2 EMUC2 EMUD3 EMUC3	I/O I/O I/O I/O I/O I/O I/O I/O	ST ST ST ST ST ST ST ST	ICD Primary Communication Channel data input/output pin. ICD Primary Communication Channel clock input/output pin. ICD Secondary Communication Channel data input/output pin. ICD Secondary Communication Channel clock input/output pin. ICD Tertiary Communication Channel data input/output pin. ICD Tertiary Communication Channel clock input/output pin. ICD Quaternary Communication Channel data input/output pin. ICD Quaternary Communication Channel clock input/output pin.
IC1, IC2, IC7, IC8	I	ST	Capture inputs 1, 2, 7 and 8.
INDX QEA QEB	I I I	ST ST ST	Quadrature Encoder Index Pulse input. Quadrature Encoder Phase A input in QEI mode. Auxiliary Timer External Clock/Gate input in Timer mode. Quadrature Encoder Phase A input in QEI mode. Auxiliary Timer External Clock/Gate input in Timer mode.
INT0 INT1 INT2	I I I	ST ST ST	External interrupt 0. External interrupt 1. External interrupt 2.
FLTA PWM1L PWM1H PWM2L PWM2H PWM3L PWM3H	I O O O O O O	ST — — — — — —	PWM Fault A input. PWM 1 Low output. PWM 1 High output. PWM 2 Low output. PWM 2 High output. PWM 3 Low output. PWM 3 High output.
MCLR	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active low Reset to the device.
OCFA OC1, OC2	I O	ST —	Compare Fault A input (for Compare channels 1, 2, 3 and 4). Compare outputs 1 and 2.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; P = Power

TABLE 1-2: dsPIC30F4012 I/O PIN DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
OSC1 OSC2	I I/O	ST/CMOS —	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
PGD PGC	I/O I	ST ST	In-Circuit Serial Programming data input/output pin. In-Circuit Serial Programming clock input pin.
RB0-RB5	I/O	ST	PORTB is a bidirectional I/O port.
RC13-RC15	8I/O	8ST	PORTC is a bidirectional I/O port.
RD0-RD1	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE5, RE8	I/O	ST	PORTE is a bidirectional I/O port.
RF2-RF3	I/O	ST	PORTF is a bidirectional I/O port.
SCK1 SDI1 SDO1	I/O I O	ST ST —	Synchronous serial clock input/output for SPI1. SPI1 Data In. SPI1 Data Out.
SCL SDA	I/O I/O	ST ST	Synchronous serial clock input/output for I^2C. Synchronous serial data input/output for I^2C.
SOSCO SOSCI	O I	— ST/CMOS	32 kHz low power oscillator crystal output. 32 kHz low power oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
T1CK T2CK	I I	ST ST	Timer1 external clock input. Timer2 external clock input.
U1RX U1TX U1ARX U1ATX	I O I O	ST — ST —	UART1 Receive. UART1 Transmit. UART1 Alternate Receive. UART1 Alternate Transmit.
VDD	P	—	Positive supply for logic and I/O pins.
VSS	P	—	Ground reference for logic and I/O pins.
VREF+	I	Analog	Analog Voltage Reference (High) input.
VREF-	I	Analog	Analog Voltage Reference (Low) input.

Legend: CMOS = CMOS compatible input or output Analog = Analog input
ST = Schmitt Trigger input with CMOS levels O = Output
I = Input P = Power

2.0 CPU ARCHITECTURE OVERVIEW

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the *dsPIC30F Family Reference Manual* (DS70046). For more information on the device instruction set and programming, refer to the *dsPIC30F Programmer's Reference Manual* (DS70030).

This document provides a summary of the dsPIC30F4011/4012 CPU and peripheral function. For a complete description of this functionality, please refer to the *dsPIC30F Family Reference Manual* (DS70046).

2.1 Core Overview

The core has a 24-bit instruction word. The Program Counter (PC) is 23 bits wide with the Least Significant (LS) bit always clear (see Section 3.1), and the Most Significant (MS) bit is ignored during normal program execution, except for certain specialized instructions. Thus, the PC can address up to 4M instruction words of user program space. An instruction pre-fetch mechanism is used to help maintain throughput. Program loop constructs, free from loop count management overhead, are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

The working register array consists of 16x16-bit registers, each of which can act as data, address or offset registers. One working register (W15) operates as a software stack pointer for interrupts and calls.

The data space is 64 Kbytes (32K words) and is split into two blocks, referred to as X and Y data memory. Each block has its own independent Address Generation Unit (AGU). Most instructions operate solely through the X memory AGU, which provides the appearance of a single unified data space. The Multiply-Accumulate (MAC) class of dual source DSP instructions operate through both the X and Y AGUs, splitting the data address space into two parts (see Section 3.2). The X and Y data space boundary is device specific and cannot be altered by the user. Each data word consists of 2 bytes, and most instructions can address data either as words or bytes.

There are two methods of accessing data stored in program memory:

- The upper 32 Kbytes of data space memory can be mapped into the lower half (user space) of program space at any 16K program word boundary, defined by the 8-bit Program Space Visibility Page (PSVPAG) register. This lets any instruction access program space as if it were data space, with a limitation that the access requires an additional cycle. Moreover, only the lower 16 bits of each instruction word can be accessed using this method.
- SWWLinear indirect access of 32K word pages within program space is also possible using any working register, via table read and write instructions. Table read and write instructions can be used to access all 24 bits of an instruction word.

Overhead-free circular buffers (modulo addressing) are supported in both X and Y address spaces. This is primarily intended to remove the loop overhead for DSP algorithms.

The X AGU also supports bit-reversed addressing on destination effective addresses, to greatly simplify input or output data reordering for radix-2 FFT algorithms. Refer to Section 4.0 for details on modulo and bit-reversed addressing.

The core supports Inherent (no operand), Relative, Literal, Memory Direct, Register Direct, Register Indirect, Register Offset and Literal Offset Addressing modes. Instructions are associated with predefined Addressing modes, depending upon their functional requirements.

For most instructions, the core is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, 3-operand instructions are supported, allowing C = A+B operations to be executed in a single cycle.

A DSP engine has been included to significantly enhance the core arithmetic capability and throughput. It features a high speed 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bi-directional barrel shifter. Data in the accumulator or any working register can be shifted up to 16 bits right or 16 bits left in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The MAC class of instructions can concurrently fetch two data operands from memory, while multiplying two W registers. To enable this concurrent fetching of data operands, the data space has been split for these instructions and linear for all others. This has been achieved in a transparent and flexible manner, by dedicating certain working registers to each address space for the MAC class of instructions.

The core does not support a multi-stage instruction pipeline. However, a single stage instruction pre-fetch mechanism is used, which accesses and partially decodes instructions a cycle ahead of execution, in order to maximize available execution time. Most instructions execute in a single cycle, with certain exceptions.

The core features a vectored exception processing structure for traps and interrupts, with 62 independent vectors. The exceptions consist of up to 8 traps (of which 4 are reserved) and 54 interrupts. Each interrupt is prioritized based on a user assigned priority between 1 and 7 (1 being the lowest priority and 7 being the highest) in conjunction with a predetermined 'natural order'. Traps have fixed priorities, ranging from 8 to 15.

2.2 Programmer's Model

The programmer's model is shown in Figure 2-1 and consists of 16x16-bit working registers (W0 through W15), 2x40-bit accumulators (AccA and AccB), STATUS register (SR), Data Table Page register (TBLPAG), Program Space Visibility Page register (PSVPAG), DO and REPEAT registers (DOSTART, DOEND, DCOUNT and RCOUNT), and Program Counter (PC). The working registers can act as data, address or offset registers. All registers are memory mapped. W0 acts as the W register for file register addressing.

Some of these registers have a shadow register associated with each of them, as shown in Figure 2-1. The shadow register is used as a temporary holding register and can transfer its contents to or from its host register upon the occurrence of an event. None of the shadow registers are accessible directly. The following rules apply for transfer of registers into and out of shadows.

- `PUSH.S` and `POP.S`
  W0, W1, W2, W3, SR (DC, N, OV, Z and C bits only) are transferred.
- `DO` instruction
  DOSTART, DOEND, DCOUNT shadows are pushed on loop start, and popped on loop end.

When a byte operation is performed on a working register, only the Least Significant Byte of the target register is affected. However, a benefit of memory mapped working registers is that both the Least and Most Significant Bytes can be manipulated through byte wide data memory space accesses.

2.2.1 SOFTWARE STACK POINTER/ FRAME POINTER

The dsPIC® devices contain a software stack. W15 is the dedicated software stack pointer (SP), and will be automatically modified by exception processing and subroutine calls and returns. However, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies the reading, writing and manipulation of the stack pointer (e.g., creating stack frames).

Note:	In order to protect against misaligned stack accesses, W15<0> is always clear.

W15 is initialized to 0x0800 during a Reset. The user may reprogram the SP during initialization to any location within data space.

W14 has been dedicated as a stack frame pointer as defined by the `LNK` and `ULNK` instructions. However, W14 can be referenced by any instruction in the same manner as all other W registers.

2.2.2 STATUS REGISTER

The dsPIC core has a 16-bit Status Register (SR), the LS Byte of which is referred to as the SR Low Byte (SRL) and the MS Byte as the SR High Byte (SRH). See Figure 2-1 for SR layout.

SRL contains all the MCU ALU operation status flags (including the Z bit), as well as the CPU Interrupt Priority Level status bits, IPL<2:0>, and the REPEAT active status bit, RA. During exception processing, SRL is concatenated with the MS Byte of the PC to form a complete word value which is then stacked.

The upper byte of the SR register contains the DSP Adder/Subtractor status bits, the DO Loop Active bit (DA) and the Digit Carry (DC) status bit.

2.2.3 PROGRAM COUNTER

The Program Counter is 23 bits wide. Bit 0 is always clear. Therefore, the PC can address up to 4M instruction words.

NOTES:

